58. (New) The flat panel display of claim 57, wherein the number of gate lines and the number of cathodes are formed using the self-aligned technique.

59. (New) The flat panel display of claim 57, wherein the number of cathodes include metal silicides on the polysilicon cones.

60. (New) The flat panel display of claim 57, wherein the number of gate lines include refractory metals.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on February 22, 2001, and the references cited therewith.

Claims 47-60 are added without any intent to introduce new matter. Applicant believes that new claims 47-60 merely express the same concept of previously pending claims 36-46 in a format apart from product-by-process. As a result, claims 36-60 are now pending in this application.

§103 Rejection of the Claims

Claims 36-46 were rejected under 35 USC § 103(a) as being unpatentable over Cloud et al. (U.S. Patent No. 5,653,619). The rejection states in relevant part:

> Cloud et al. further disclose that a distance separating the number of cathode emitter tips from the number of gate lines is significantly thinner than a separation distance separating the number of gate lines and the substrate (see Fig 1, Fig 2, and Fig 2B).

The rejection further states that:

> Cloud also teaches that "the insulating layer 18 can be deposited to a level below the tip 13, as shown in Fig. 2. Alternatively, insulating layer 18 can be deposited to a level substantially equal to or slightly higher than the level of the cathode emitter 13 as shown in Fig. 2A and Fig. 2B" (see lines 51-55 of column 5). Thus as disclosed by Cloud, the insulating layer is not constant over the entire region of the substrate 11.

The process of Cloud states that the insulating layer is "preferably a conformal insulating layer" (col. 5, ln. 62). A conformal layer possesses a substantially uniform thickness as it conforms to features it is deposited over, such as the cathode 13 in the Cloud reference. The Cloud reference also appears to discuss a careful process of choosing a uniform thickness for the conformal insulating layer in column 5, lines 44-50.

> Hence, the insulating layer 18 must be as thin as possible, since small gate 15 to cathode 13 distances result in lower emitter drive voltages, at the same time, the insulating layer 18 must be large enough to prevent the oxide breakdown which occurs if the gate is not adequately spaced from the cathode conductor 12.

Cloud **does not teach *variations* in thickness** of the insulating layer 18. It merely teaches that the single uniform thickness chosen must be chosen with certain performance factors in mind as discussed in the Cloud quotation above. In fact, Cloud teaches away from varying the thickness of the insulating layer 18 as cited by the Examiner when Cloud states that the insulating layer is **preferably** conformal.

A gate layer 15 appears to be deposited over the preferably conformal insulating layer 18. Because the preferably conformal insulating layer is uniform in thickness, and no material has been removed from the insulating layer, the distance separating the gate lines from the substrate is equal to the uniform thickness of the insulating layer. Because the thickness of the insulating layer is uniform, it is impossible for any portion of the gate layer 15 to be closer to the cathode 13 than the distance separating the gate lines from the substrate.

The Cloud reference appears to show an embodiment where the distance separating the gate lines from the substrate is thin such that the level of the insulating layer is below the tip of cathode 13. Cloud also appears to show an embodiment where the distance separating the gate lines from the substrate is thicker such that the level is substantially equal to or slightly higher than the tip of the cathode 13. In both cases, however, **the distance separating the gate lines from the substrate is substantially the same distance as the closest spacing between the cathode emitter tips and the number of gates lines because the thickness of the insulating layer is uniform**.

In contrast, Applicant's invention includes a field emitter array where the distance separating the number of cathode emitter tips from the number of gates lines is significantly

thinner than a separation distance separating the number of gate lines and the substrate.

The process of the invention begins with an insulator layer that is uniform in thickness. However, Applicant's novel process then preferentially removes a portion of the insulator layer (page 8, lines 5-13, Figure 1C), creating a **non-uniform thickness insulator layer** 102. The insulator layer in Applicant's invention is thinner in a region near the cathode tip 101, and thicker in all other regions that will determine a distance separating the gate lines from the substrate. Therefore, when the gate layer 116 is deposited over the non-uniform thickness insulator layer of Applicant's invention, it is possible to have a distance separating the number of cathode emitter tips from the number of gates lines that is significantly thinner than a separation distance separating the number of gate lines and the substrate

As a direct result of utilizing Applicant's novel process to create a non-uniform thickness insulator layer, Applicant's product is unique and patentably distinct from the product in Cloud. Reconsideration and withdrawal of Examiner's 35 USC § 103(a) rejection is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JI UNG LEE

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 23 day of April, 2001.

Tina Pugh
Name

Signature